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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/834,751	04/13/2001	Sergey A. Velichko	303.750US1	4280

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EXAMINER	
BARBEE, MANUEL L	
ART UNIT	**PAPER NUMBER**
2857	

DATE MAILED: 01/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/834,751	VELICHKO ET AL.	
	Examiner	Art Unit	
	Manuel L. Barbee	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

On page 8, line 24, delete "sate", and insert --state--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-9, 16-22, 29-37 and 44-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ekstedt et al. (US Patent No. 5,206,582) in view of Chen et al. (US Patent No. 5,726,920).

With regard to a control module operable to control operation of semiconductor test equipment and operation of parametric test instrumentation, as shown in claims 1, 16, 29 and 44, Ekstedt et al. teach a controller that is used to control a wafer prober and measurement instruments (col. 3, line 42 - col. 4, line 58; col. 10, lines 15-61; Fig. 1, controller 16, wafer prober 13, measurement instruments 10; Figs. 8, 9). Ekstedt et al. do not teach concurrent operation of semiconductor test equipment and operation of parametric test equipment. Chen et al. teach that wafer electrical testing (WET) occurs along the movement path as a wafer is moved from a transport cassette to final wafer sort test station (col. 5, lines 49-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the control system, as taught by

Ekstedt et al., to include performing a test while the wafer is being moved, as taught by Chen et al., because the economic well-being of the wafer production would have been improved by faster testing (Chen et al., col. 3, lines 46-54).

With regard to implementing the control module in software and in electronic hardware, as shown in claims 2, 3, 30, 31, 45 and 46, Ekstedt et al. teach a desktop computer that may run software to control testing (col. 4, lines 7-58; Fig. 2; col. 3, line 60 - col. 4, line 6). With regard to wafer positioner and a prober, as shown in claims 4, 17, 32 and 47, Ekstedt et al. teach a wafer prober and a positioning mechanism (col. 3, lines 42-60; Fig. 1, wafer prober 13, positioning mechanism 17). With regard to a test probe or test receptacle, as shown in claims 5, 18, 33 and 48, Ekstedt et al. teach probe card and relay matrix connected to the measurement instruments (Fig. 1, probe card 14, relay matrix 12, measurement instruments 10). With regard to a test equipment module, as shown in claims 6, 19, 34 and 49, and a test instrumentation module, as shown in claims 7, 20, 35 and 50, Ekstedt et al. teach control software with routines for positioning the prober and algorithms for performing the tests (col. 4, lines 43-58). With regard to operating a semiconductor test parameter module, as shown in claims 8, 21, 36 and 51, Ekstedt et al. teach control software with algorithms for performing the tests (col. 4, lines 43-58). With regard to concurrently managing test data, as shown in claims 9, 22, 37 and 52, Ekstedt et al. teach managing the variables for test parameters and the test results (col. 8, lines 40-66; col. 11, line 36 - col. 12, line 19).

4. Claims 10-15, 23-28, 38-43 and 53-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ekstedt et al. in view of Chen et al. as applied to claims 1, 16, 29 and 44 above, and further in view of Gloudeman et al (US Patent No. 6,119,125).

Ekstedt et al. and Chen et al. teach all the limitations of claim 1 upon which claims 10-13 depend, claim 16 upon which claims 23-28 depend, claim 29 upon which claims 38-43 depend and claim 44 upon which claims 53-58. Further with regard to an abort superstate, a pause superstate and a lot run superstate, as shown in claims 13, 26, 41 and 56, Ekstedt et al. teach exiting the testing loop when a defective device is found, pausing for user input and the normal testing routine (col. 11, line 4-35; col. 10, lines 32-51).

Ekstedt et al. and Chen et al. do not teach a state oscillator module to provide fault-tolerant control of the test state, as shown in claims 10, 23, 38 and 53, or a state oscillator module that changes the state of other system modules, as shown in claims 11, 24, 39 and 53, or controlling the operation of the state oscillator module in synchronization with other system events, as shown in claims 12, 25, 40 and 54. Gloudeman et al. teach a Simple Finite State Machine (SFSM) that is an event controller, which changes states based on rules, supports the implementation of a hierarchical state diagram (col. 16, line) 51 - col. 17, line 47). The SFSM uses events and inputs to control the state change and synchronize operation with other components (col. 16, lines 51-58; col. 17, lines 39-47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the control system combination, as taught by Ekstedt et al. and Chen et al., to include the SFSM,

as taught by Gloudeman et al., because then the operation of different software components together would have been facilitated (Gloudeman et al., col. 1, lines 19-37).

Claims 14, 27, 42 and 57 contain limitations similar to those found in claims 1, 6, 7 and 10 and are rejected on the same grounds. Claims 15, 28, 43 and 58 contain limitations similar to those found in claims 1, 2, 4-8 and 10 and are rejected on the same grounds.

Response to Arguments

5. Applicant's arguments with respect to claims 1-58 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Manuel L. Barbee whose telephone number is 571-272-2212. The examiner can normally be reached on Monday-Friday from 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Manuel L. Barbee
Examiner
Art Unit 2857

mlb
January 20, 2006